



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

09/123,450

07/28/98

TATEL

D

10065, 07/27/98

MM91/0418

THOMAS J D AMICO
DICKSTEIN SHAPIRO MORIN AND OSHINSKY
2101 L STREET N W
WASHINGTON DC 20037-1526

EXAMINER

REDELEB

ART UNIT

PAPER NUMBER

3823

DATE MAILED:

04/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/123,430

Applicant(s)

YATES, DONALD L.

Examiner

Brook Kebede

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 February 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 and 48-60 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13 and 23 is/are allowed.
- 6) ☒ Claim(s) 1-12, 14-22, 24-27 and 48-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 18) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on October 4, 2000 in Paper No. 11 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "a non-uniform flow rate" in claims 1, 7, 17, and 44; "non-constant velocity" in claim 25. Applicant is required to cancel the new matter in the reply to this Office Action.
2. The amendment filed on February 21, 2001 in Paper No. 17 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "the velocity of said portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value" in claims 48-60. Applicant is required to cancel the new matter in the reply to this Office Action

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
4. Claims 1-10, 16, 17-20, 25, 26, 27, 44 and 48-60 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. .

Art Unit: 2823

Re claims 1, 7, 17 and 44, the claimed limitation “a non-uniform flow rate” has no support in the specification as originally filed. Therefore, the claimed limitation “a non-uniform flow rate” does not contain a written description of the invention in full, clear concise manner as required by first paragraph of 35 USC § 112.

Re claim 25, the claimed limitation “a non-uniform velocity” has no support in the specification as originally filed. Therefore, the claimed limitation “a non-uniform velocity” does not contain a written description of the invention in full, clear concise manner as required by first paragraph of 35 USC § 112.

Re claims 48-60, the claimed limitation “the velocity of said portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value” has no support in the specification as originally filed. Therefore, the claimed limitation “the velocity of said portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value” does not contain a written description of the invention in full, clear concise manner as required by first paragraph of 35 USC § 112.

Claims 2-6, 8-10, 16, 18-20, 26 and 27 are rejected as being dependent of the rejected base claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9, 14, 17-20, 24, 26, 44, 48, 49 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al., (USPAT/5,275,184).



Re claim 1, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers the method comprising rapidly removing at non-uniform flow rate an upper portion semiconductor processing fluid present in the bath while the wafers are in the bath (see Fig. 2 and Col. 2, lines 62-67 through Col. 5, lines 1-27).

Re claims 2 and 3, as applied to claim 1 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the semiconductor process bath as an etching/cleaning bath (see Fig. 2 and abstract).

Re claim 4, as applied to claim 1 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the contaminants are removed from the air/liquid interference of the semiconductor processing bath (see Fig. 2)

Re claim 5, as applied to claim 4 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the semiconductor process bath as an etching bath (see Fig. 2 and abstract).

Re claim 6, as applied to claim 1 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the contaminants include silica (see Fig. 2).

Re claim 7, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from wet etching bath comprising: processing the semiconductor wafer in the wet etching bath containing and etching fluid; subsequently rapidly removing at non-uniform flow rate an upper portion of the etching fluid from the wet etching bath to remove contaminants from the surface of the wet etching bath while retaining the semiconductor wafer in the etching bath and subsequently removing of the wafer from the bath (see Fig. 2 and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

Art Unit: 2823

Re claim 8, as applied to claim 7 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein substantial etching fluid (see Fig 2 and related text in Col. 3, lines 17-23).

Re claim 9, as applied to claim 8 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the upper portion of the etching fluid is removed by draining a top portion of the etching fluid from wet etching bath (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 14, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath while the wafers are in the bath by rapidly removing a wafer boat containing the semiconductor wafer from the bath (see Fig. 2).

Re claim 17, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel at non-uniform flow rate while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

Re claim 18 as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the semiconductor is a silicon wafer (see abstract)

Re claim 19 as applied to claim 18 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is an aqueous HF solution (see related text in Col. 11, lines 18-20).



Re claim 20, as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from an upper surface of the wet etching vessel by draining of the top portion of the etching fluid from the wet etching vessel (see Fig. 2 and related text in Col. 7, lines 2-14).

Re claim 24, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel by rapidly removing a wafer boat containing the semiconductor wafers from the wet etching vessel (see Fig. 2).

Re claim 26, as applied to claim 17 above, Nishizawa et al. disclose all the claimed limitations including the limitation wherein the etching fluid is removed from the upper surface of the wet etching vessel by physically removing a top portion of the etching fluid from the wet etching bath (see Fig. 2).

Re claim 44, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: immersing a wafer boat in an etching vessel having an etching fluid therein for sufficient time to etch the silicon wafer; and rapidly removing the wafer boat from the etching vessel to remove the contaminants residing on the upper surface of the etching fluid by causing the etching fluid to spill out of the vessel at a non-uniform flow rate (see Fig. 2).

Re claim 48, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers, said method comprising: removing an upper portion of a semiconductor processing fluid present in said bath from said while said wafers are in said bath, in a manner such that the velocity of said upper portion of said



Art Unit: 2823

semiconductor processing fluid rapidly increases at the point of removal from a first value to a second higher value (see Fig. 2).

Re claim 49, Nishizawa et al. disclose a method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising: processing said semiconductor wafer in said wet etching bath containing an etching fluid; subsequently suddenly removing an upper portion of said etching fluid from said wet etching bath to remove contaminants from the surface of said wet etching bath while retaining said semiconductor wafer in said wet etching bath, in a manner such that the velocity of said upper portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value; and subsequently removing said semiconductor wafer from said wet etching bath (see Fig. 2)

Re claim 55, Nishizawa disclose a method for etching a semiconductor wafer, said method comprising: placing an etching fluid into a wet etching vessel; placing said semiconductor wafer in said etching fluid; contacting said semiconductor wafer with said etching fluid for a predetermined time; removing a portion of said etching fluid from the upper surface of said wet etching vessel while keeping said semiconductor wafer immersed in said etching fluid, in a manner such that the velocity of said portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value; and removing said semiconductor wafer from said etching fluid (see Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.



Art Unit: 2823

8. Claims 10, 16 and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al., USPAT/5,275,184 in view of Itoh et al., USPAT/5,795,401.

Re claims 10 and 16, Nishizawa et al. teach all the limitation in the claimed limitations as applied in claim 7 except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

Re claim 27, Nishizawa et al. teach all the limitation in the claimed invention as applied in claim 26 except the use of paddle to remove the fluid from the top portion of the etching process bath.

Itoh et al. disclose the use of back paddle to jet (remove) out the wash fluid during process of cleaning of semiconductor substrate (see related text in Col. 10, lines 18-48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with paddle as taught by Itoh et al. because the use of paddle would have provided removing of contaminants from the top of the wafer etching bath.

9. Claims 11, 21, 50 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al., USPAT/5,275,184 in view of Mohindra et al., USPAT/5,958,146.

Re claim 11, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers the method comprising:

Art Unit: 2823

rapidly removing an upper portion of a semiconductor processing fluid presented in the bath, while the wafer in the bath (see Fig. 2). Although, the process is inherent, Nishizawa et al. do not mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided another method of removing contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 21, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing an etching fluid into a wet etching vessel; placing the semiconductor wafer in the etching fluid; contacting the semiconductor wafer with the etching fluid for a period of time; and rapidly removing a portion of the etching fluid from the upper surface of the wet etching vessel (see Fig. 2). Although, the process is inherent, Nishizawa et al. do not mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 50, Nishizawa et al. disclose a method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers, said method comprising

Art Unit: 2823

removing an upper portion of a semiconductor processing fluid present in said bath, while said wafers are in said bath in a manner such that the velocity of said upper portion of said semiconductor processing fluid rapidly increases at the point of removal from a first value to a second higher value (see Fig. 2). Although, the process is inherent, Nishizawa et al. do not mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

Re claim 56, Nishizawa et al. disclose a method for etching a semiconductor wafer, said method comprising: placing an etching fluid into a wet etching vessel; placing said semiconductor wafer in said etching fluid; contacting said semiconductor wafer with said etching fluid for a predetermined time; and removing a portion of said etching fluid from the upper surface of said wet etching vessel in a manner such that the velocity of said portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value (see Fig. 2). Although, the process is inherent, Nishizawa et al. do not mention use of valve to remove the etching fluid.

Mohindra et al. disclose the use of valve to remove during cleaning (etching) process of the semiconductor wafer (see related text in Col. 3, lines 56-60).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a valve

Art Unit: 2823

as taught by Mohindra et al. because the use of valve would have provided removing of contaminants from the top of the wafer etching bath when the valve opens by mechanical means.

10. Claims 12, 15, 22, 25, 51, 54, 57 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (USPAT/5,275,184) in view of Hayami et al. (USPAT/5,474,616).

Re claim 12, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing bath for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 15, Nishizawa et al. disclose a method of removing contaminants from a semiconductor processing bath for processing semiconductor wafers the method comprising: rapidly removing an upper portion of a semiconductor processing fluid present in the bath, while the wafers are in the bath (see Fig. 2). However, Nishizawa et al. do not disclose removing a



portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 22, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14).

However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have

Art Unit: 2823

provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 25, Nishizawa et al. disclose a method for etching a semiconductor wafer the method comprising: placing and etching fluid into a wet etching vessel; placing the semiconductor fluid into wet etching fluid; contacting the semiconductor wafer with the etching fluid for period or time; rapidly removing a portion of the etching fluid from the upper surface of wet etching vessel at a non-constant velocity while keeping the semiconductor wafer immersed in the etching fluid (see Fig. 2, and related text in Col. 2, lines 62-67 through Col. 5, lines 1-27; Col. 20, lines 7-14). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 51, Nishizawa disclose a method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers, said method comprising removing an upper portion of a semiconductor processing fluid present in said bath, while said wafers are in said bath, by hingedly releasing a door located at an upper portion of said bath in a manner such that the velocity of said upper portion of said semiconductor processing fluid

Art Unit: 2823

rapidly increases at the point of removal from a first value to a second higher value (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 54, Nishizawa et al. disclose method for removing contaminants from a semiconductor processing bath for processing semiconductor wafers, said method comprising removing an upper portion of a semiconductor processing fluid present in said bath, while said wafers are in said bath in a manner such that the velocity of said upper portion of said semiconductor processing fluid rapidly increases at the point of removal from a first value to a second higher value (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath. (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a



Art Unit: 2823

hingedly released door as taught by Hayami et al. because the use of telescopically collapsing sidewalls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Re claim 57, Nishizawa disclose a method for etching a semiconductor wafer, said method comprising: placing an etching fluid into a wet etching vessel; placing said semiconductor wafer in said etching fluid; contacting said semiconductor wafer with said etching fluid for a predetermined time; and removing a portion of said etching fluid from the upper surface of said wet etching in a manner such that the velocity of said portion of said etching fluid rapidly increases at the point of removal from a first value to a second higher value (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by hingedly releasing a door located at an upper portion of the bath (see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of the door would have provided removing of contaminants from the top of the wafer etching bath when the door opened.

Re claim 60, Nishizawa disclose a method for etching a semiconductor wafer, said method comprising: placing an etching fluid into a wet etching vessel; placing said semiconductor wafer in said etching fluid; contacting said semiconductor wafer with said etching fluid for a predetermined time; and removing a portion of said etching fluid from the upper surface in a manner such that the velocity of said portion of said etching fluid rapidly increases at



Art Unit: 2823

the point of removal from a first value to a second higher value (see Fig. 2). However, Nishizawa et al. do not disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.

Hayami et al. disclose removing a portion of the etching fluid from upper surface of the etching bath, by telescopically collapsing sidewalls of the vessel containing the bath.
(see Fig. 41 and 42).

Therefore, it would have been obvious to one ordinary skill in the art at the time of applicant's claimed invention was made to have provided Nishizawa et al. reference with a hingedly released door as taught by Hayami et al. because the use of telescopically collapsing side-walls would have provided removing of contaminants from the top of the wafer etching bath when the sidewall folded.

Allowable Subject Matter

11. Claims 13 and 23 are allowed over prior art of record.
12. Claims 52, 53, 58 and 59 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office action.

Response to Arguments

13. Applicant's arguments with respect to claims 1-27 and 48-60 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. This Office action is **made NON-FINAL**.

Correspondence

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

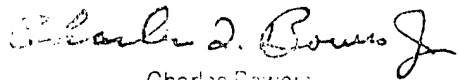
Art Unit: 2823

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

17. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
April 17, 2001



Charles Ewers
Supervisory Patent Examiner
Technology Center 2800